IN THE CLAIMS

The listing of claims replaces all prior versions, and listings, of claims in the application. Please amend the claims as follows:

1. (Currently amended) A computer peripheral device comprising:

a memory for storing a configuration address; and

[[a]] an independent power level control circuit for controlling the power level in the device so as to be in a standby mode or normal power mode after power is applied to the device, the circuit being coupled to the memory to control an initial assignment of ~~cause the memory to store the~~ configuration address from a bus to the memory when the ~~device~~ circuit enters the normal power mode after it is activated by a software application.

2. (Previously presented) The device defined by claim 1 wherein the memory, once storing a configuration address, retains that address until the device is reset or the power is turned on or off.

3. (Previously presented) The device defined by claim 1 wherein the memory does not change its stored address when the device is reconfigured.

4. (Currently amended) The device defined by claim ~~3~~ 1 wherein the bus is an address bus.

5. (Previously presented) The device defined by claim 4 wherein the memory restores an address after a reset signal is received by the circuit or the power is turned on or off.

6. (Original) The device defined by claim 5 wherein the circuit is responsive to two addresses once a configuration address is stored.

7. (Previously presented) The device defined by claim 1 wherein the memory restores an address after a reset signal is received by the circuit or the power is turned on or off.

8. (Currently amended) A computer system comprising:

a processor; and

a plurality of peripheral devices coupled to the processor through at least one bus, each device having [[a]] an independent power level control circuit for controlling the power level in the device ~~causing the device~~ to be in a standby mode or normal ~~operating~~ power mode once power is applied to the device and for controlling the initial assignment of a configuration address, and a ~~storage circuit~~ memory for storing the configuration address~~, the storage circuit storing~~ from the bus upon being enabled by a signal from the circuit after it is activated by a software application into the normal power mode. ~~a configuration address from the bus when the power level control circuit initially causes the device to be in the normal operating mode.~~

9. (Original) The system defined by claim 8 wherein the bus is an address bus.

10. (Previously presented) The system defined by claim 8 wherein each of the peripheral devices is initially sequentially brought into a normal operating mode from a standby mode.

11. (Previously presented) The system defined by claim 10 wherein the peripheral devices are sequentially brought into the normal operating mode after a reset or after power is turned on or off.

12. (Currently amended) A computer system comprising:

a processor;

an output unit coupled to the processor; and

a plurality of peripheral devices each ~~being coupled to a bus and~~ controlled by a power level circuit ~~being~~ coupled to a power level control line from the output unit, signals over each control line causing each ~~device~~ circuit to be placed in a standby mode or normal ~~operating~~ power mode after power is applied to the device, each peripheral device having a memory coupled to at least one bus which receives and stores a configuration address from the bus in response to a controlling ~~the~~ signal ~~on its respective power level control line~~ from the circuit which causes the ~~device~~ circuit to enter its normal ~~operating~~ power mode upon activation of the circuit by a software application.

13. (Original) The system defined by claim 12 wherein the bus is coupled between the output unit and the peripheral devices.

14. (Original) The system defined by claim 13 wherein the bus is an address bus.

15. (Previously presented) The system defined by claim 12 wherein the memory of each of the peripheral devices store a configuration address only when first entering the normal operating mode after a reset or after the power is turned on or off.

16. (Previously presented) A method for operating a computer system comprising:

applying power to a plurality of peripheral devices;

entering a power standby mode in the plurality of peripheral devices;

sequentially entering a normal power mode from the standby mode for each of the peripheral devices; and

storing a unique configuration address in each device only when initiated by a signal from a power level control circuit, as each circuit enters the normal power mode after being activated by a software application.

17. (Original) The method defined by claim 16 wherein the storing step occurs after reset.

18. (Previously presented) The method defined by claim 16 wherein the storing step for each peripheral device includes the reading of data from a bus.

19. (Previously presented) The method defined by claim 18 wherein the reading of data from a bus comprises the reading of data from a data bus and an address from an address bus.

20. (Original) The method defined by claim 18 including configuring each peripheral device after it has stored its configuration address.